INFORMATION DISCLOSURE STATEMENT BY APPLICANT PTO-1449 FORM	ATTY. DOCKET NO. 10746/32	U.S. SERIAL NO. 10/092,089
	APPLICANT KISHINE et al.	
	FILING DATE March 5, 2002	GROUP 2859

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
LW	06252654	September 9, 1994	Japan	—	—	X	
LW	11055082	February 26, 1999	Japan	—	—	X	
LW	10126400	May 15, 1998	Japan	—	—	X	

* Copy of reference is not enclosed because reference is cited and described in Search Report (copy of reference provided by International Searching Authority).

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EXAMINER INITIAL		AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
LW		Noboru Ishihara, Yukio Akazawa, "A Monolithic 156 Mb/s Clock and Data Recovery PLL Circuit Using the Sample-and-Hold Technique", IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 29, NO. 12, DECEMBER 1994, pp. 1566-1571.
LW		D. Clawin, U. Langmann, "Multigigabit/second Silicon Decision Circuit", ISSCC 85, February 1985, pp.222-223.
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EXAMINER	DATE CONSIDERED 10/3/05

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT PTO-1449 FORM	ATTY. DOCKET NO. 10746/32	U.S. SERIAL NO. 10/092,089
	APPLICANT KISHINE et al.	
	FILING DATE March 5, 2002	GROUP 2634

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE*

FOREIGN PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
LW	10-285150	October 23, 1998	Japan	—	—	Abstract	

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LW		Müllner et al., "A 20 Gbit/s Parallel Phase Detector and Demultiplexer Circuit in a Production Silicon Bipolar Technology with f_T=25 GHz", BIPOLAR/BICMOS Circuits and Technology Meeting, IEEE, 29 September 1996, pp. 43-45.
LW		J. Savoj, B. Razavi, "A 10 Gb/s CMOS Clock and Data Recovery Circuit", 2000 Symposium on VLSI Circuits Digest of Technical Papers, pp.136-139.
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EXAMINER [signature] DATE CONSIDERED 5/4/06

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SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT BY APPLICANT	ATTY. DOCKET NO. 10746/32	U.S. SERIAL NO. 10/092,089
	APPLICANT Keiji KISHINE et al.	
	FILING DATE March 5, 2002	GROUP 2859

U. S. PATENT DOCUMENTS

EXAMINER INITIAL	PATENT NUMBER	PATENT DATE	NAME	CLASS	SUBCLASS	FILING DATE*
LW	6,259,755	July 10, 2001	Eugene O'Sullivan et al.			

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EXAMINER INITIAL	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
LW	5-56410	March 5, 1993	Japan			Abst.	

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LW		M. Wurzer et al., "A 40-Gb/s Integrated Clock and Data Recovery Circuit in a 50-GHz Silicon Bipolar Technology, "IEEE J. Solid-State Circuits, Vol. 34, No. 9, pp.1320-1324 Sep. 1999.

EXAMINER	DATE CONSIDERED 10/3/05

EXAMINER: Initial if citation considered, whether or not citation is in conformance with M.P.E.P. 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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